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Prof. Tien-Sheng Chao / Department of Electrophysics

- Office：SC306
- Lab：SC704 Advanced Semiconductor Fabrication and Measurement Laboratory
- Educational Background
  - —B.A., Electronics Engineering, 1985, National Chiao Tung University, Taiwan
  - —Ph.D., Electronics Engineering, 1992, National Chiao Tung University, Taiwan
- Working Experience

Researcher	1992-2001	National Nano Device Laboratories, Taiwan
Associate Professor	1997-2001	Engineering and System Science, National Tsing Hua University, Taiwan
Associate Professor	2001-2002	Department of Electrophysics, National Chiao Tung University, Taiwan
Vice-Chairman	2002-2004	National Nano Device Laboratories, Taiwan
Chairman	2009-2011	Department of Electrophysics, National Chiao Tung University, Taiwan
Professor	2002-	Department of Electrophysics, National Chiao Tung University, Taiwan

- Research Expertise
  - —Semiconductor Physics and Devices
  - —Integrated Circuit Technology
  - —Thin film transistors
  - —Nano Devices

Achievements

A. **Poly-Si short channel gate-all-around (GAA) junctionless transistor (JL-FET)** compared favorably with single-crystal devices, having subthreshold swing close to ideality and operating under 1 volt. (Fig. A)

B. **3D-stack applicable, strained channel-sidewall damascened trigate poly-S JL FinFET** which could avoid the limitation of stress liner thickness of deep-submicron MOSFETs. (Fig. B)

C. **3D vertical stack multi-channel nano-belt junctionless transistor** with high conducting current. (Fig. C)

D. **Shell-doping profile junctionless transistor** with low off-current and low subthreshold swing. (Fig. D)

E. **Novel poly-Si Tunnel FET** with low power and low temperature process. (Fig. E)

Fig. A-1.

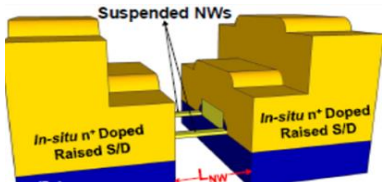

Fig. A-2.

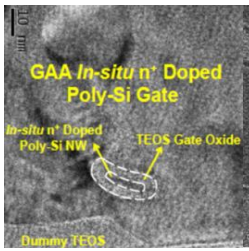

Fig. B.

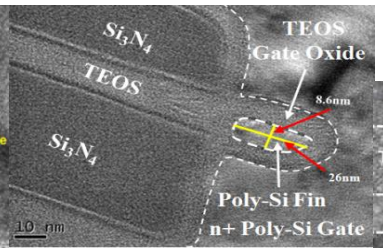

Fig. C.

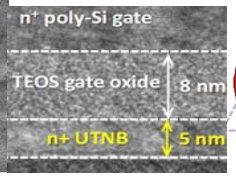

Fig. D.

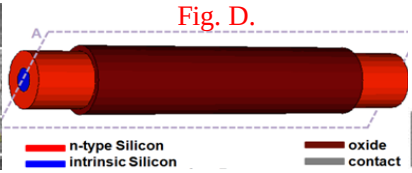

Fig. E.